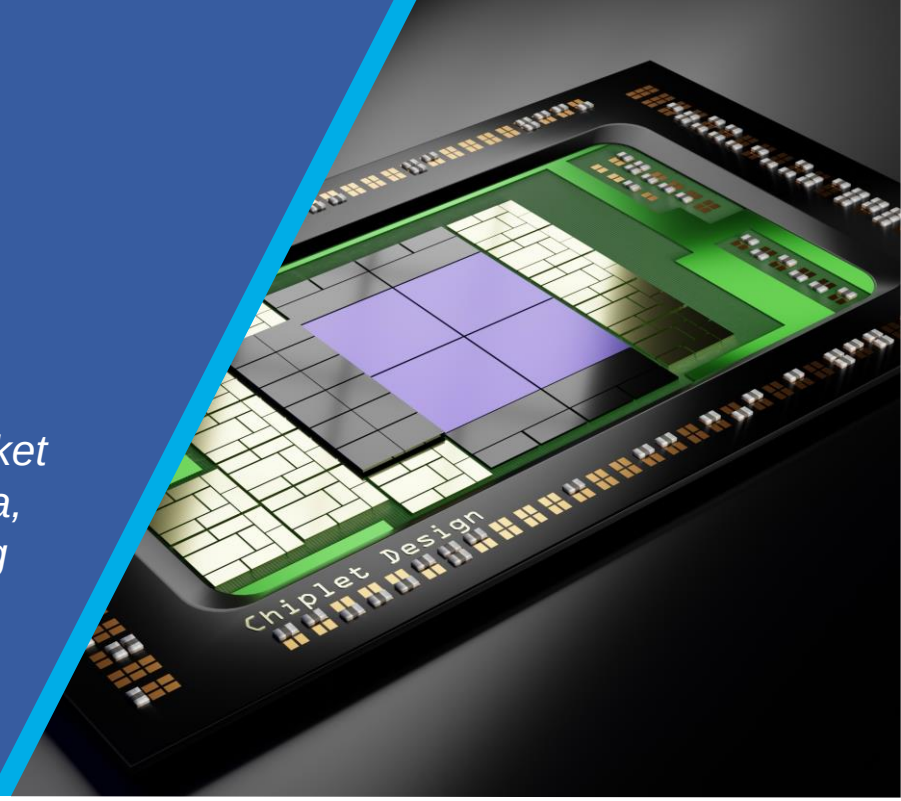
Advanced Semiconductor Packaging 2025-2035: Forecasts, Technologies, Applications

Heterogeneous Integration, AI, HPC, Data Centers, Semiconductor Packaging Market Forecast, Antenna in Package, 2.5D, 3D, Fan-Out, FOWLP, FOPLP, Through-Si-Via, Glass Packaging, Co-Packaged Optics, RDL (Redistribution Layer), Hybrid Bonding

Dr Yu-Han Chang, Principal Technology Analyst
Dr James Jeffs, Principal Technology Analyst



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Report Overview

Slides:	530
Forecasts to:	2035
Companies:	18

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25% CAGR is forecast for the growth of advanced semiconductor packaging in the HPC sectors.

Advanced Semiconductor Packaging 2025-2035: Forecasts, Technologies, Applications

IDTechEx's "Advanced Semiconductor Packaging 2025-2035" report delves into the evolving semiconductor packaging landscape, with a focus on 2.5D and 3D packaging technologies. It examines current technology trends, industry challenges, and the advancements of key players, while also forecasting future market trends. Utilizing IDTechEx's expertise in AI, data centers, autonomous vehicles, 5G, and consumer electronics, the report provides a thorough understanding of how advanced semiconductor packaging is influencing these sectors, offering valuable insights into the industry's future trajectory.

This report includes:

- An exploration of technology trends and manufacturers in advanced semiconductor packaging.
- 10-year granular market forecasts & analysis.
- An examination of the adoption of key advanced semiconductor packaging technologies (including 2.5D embedded Si, 2.5 Si interposer, 2.5D (Ultra) high density fanout, and 3D die stacking) in the four primary markets (Data Centers, Autonomous Vehicles, 5G, Consumer Electronics) studied by IDTechEx.

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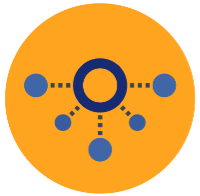

Track the competition

Save time and resources

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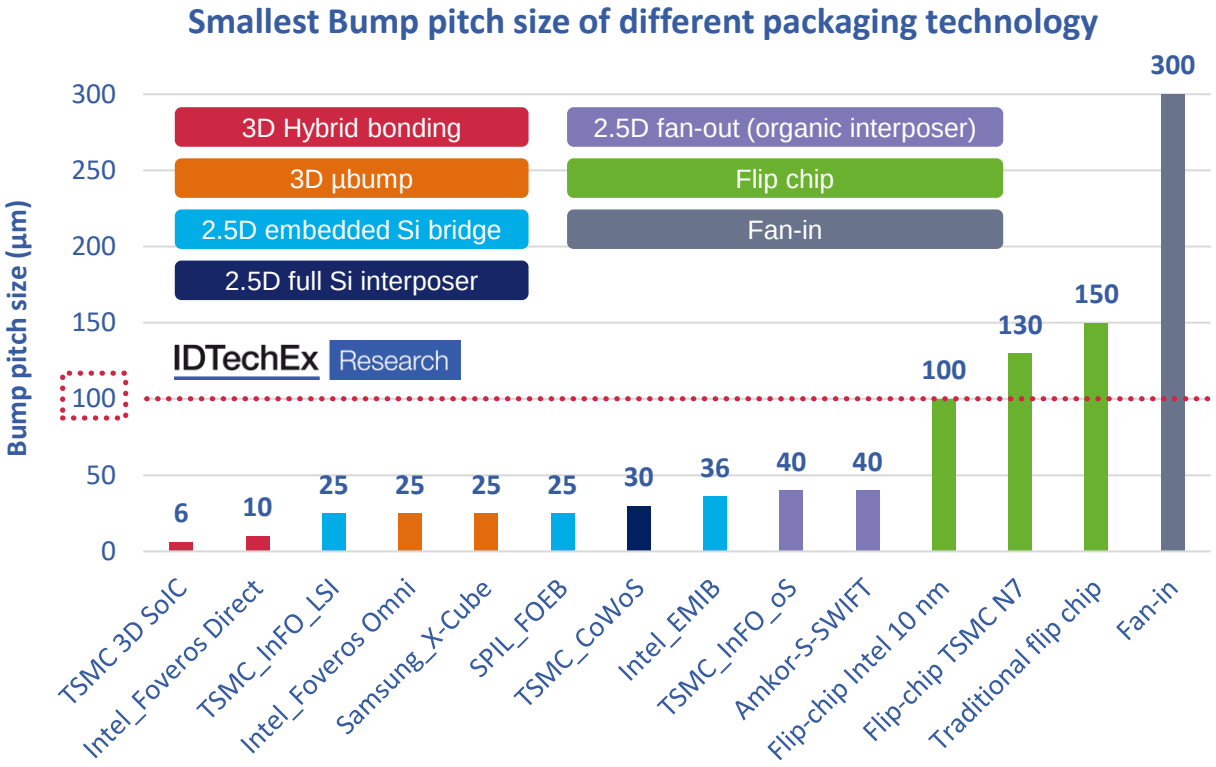
Advanced semiconductor packaging technologies – our scope

The first semiconductor package was invented in 1965, since then packaging technologies have been developing. Now, there are many packaging technologies, ranging from the most widely used wire bond to the most advanced 3DICs. What technologies are categorized as advanced semiconductor packaging? One approach to categories is by bump pitch size. The smaller bump pitch size means more I/O counts which translates to higher interconnection densities, which is required in many high-computing applications. Below, the chart shows the smallest bump pitch size of different packaging technologies offered by different companies. In this report, we define "advanced semiconductor packaging" as any package with a bump size of less than 100 µm.



I/O increases with decreasing bumping size

For example: A 10 µm bumping size packaging technique can offer about 400 times the I/O counts as 200 µm bumping size packaging technology.

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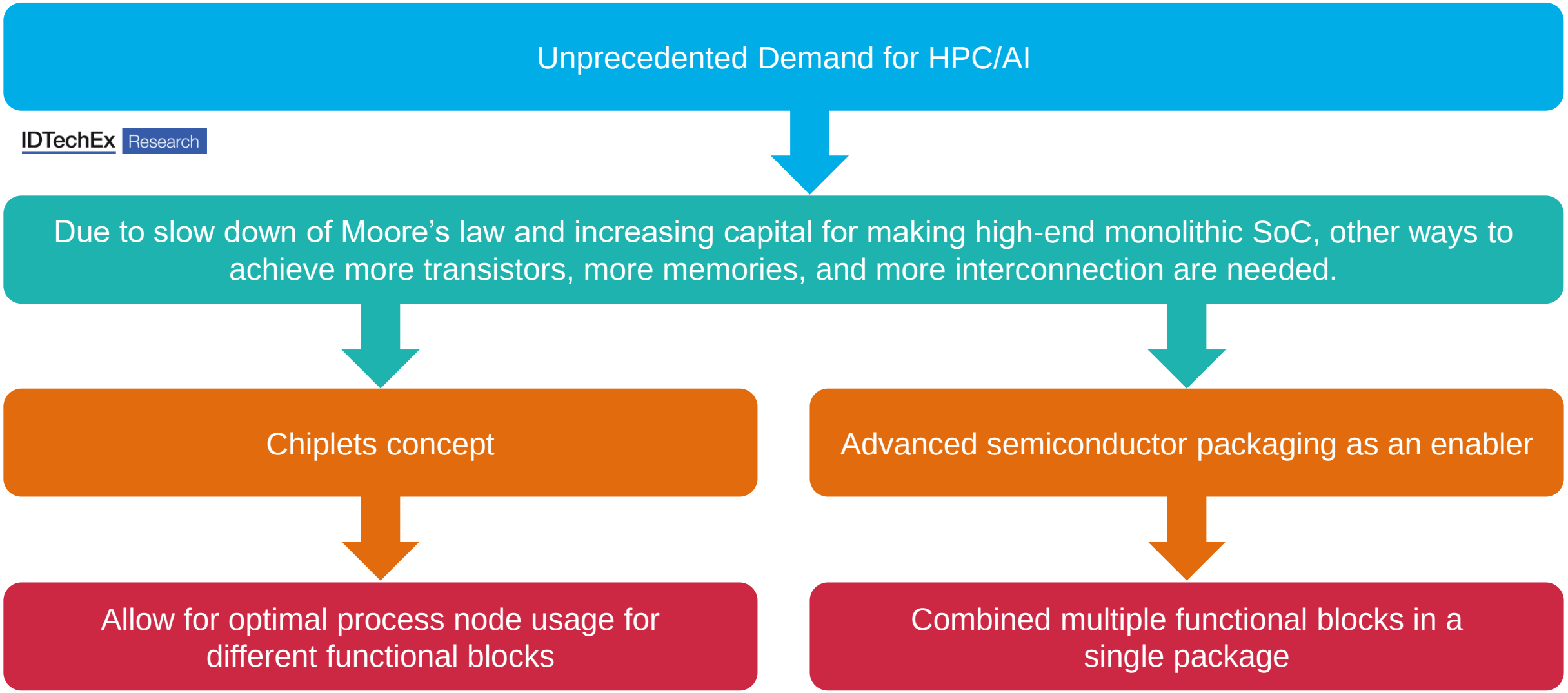
Why advanced semiconductor packaging now?



Evolution roadmap of semiconductor packaging

1D → **2D** → **2D enhanced (2.1D – 2.5D)** → **3D**

Board level integration

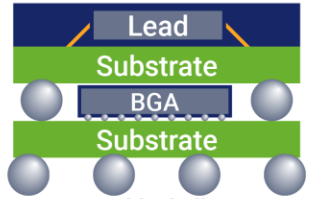
Different packaged chips assembled on a PCB board

Package level integration

Integration of different packages/components on a unifying substrate

Multi-chip Module (MCM)

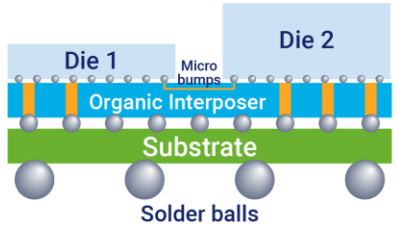
Package on package (PoP)



Wafer level integration

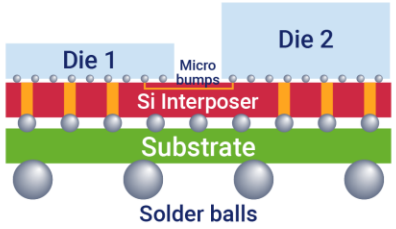
Organic interposer

Integration of different dies on an organic interposer/redistribution layer (RDL) and packaged on a unifying substrate

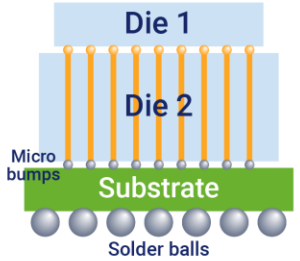


Si interposer

Integration of different dies on a Si interposer or Si bridge (i.e., inactive dies) and packaged on a unifying substrate



Integration of different active dies on top of each other and packaged on a unifying substrate



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Low → **High**

Interconnect density, Level of application,
Cost, Process challenges

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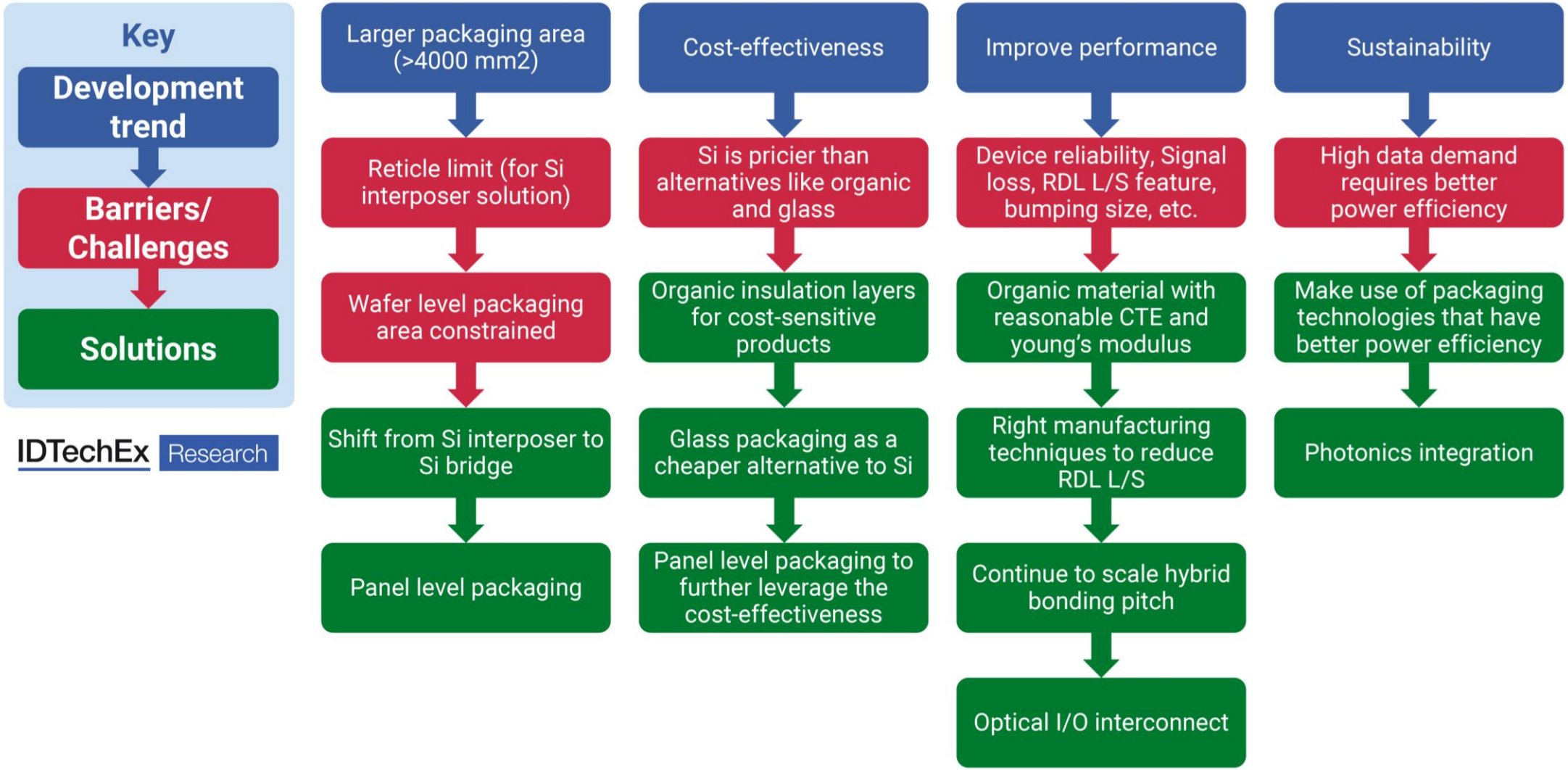
Tech development trend for 2.5D and 3D packaging



Advanced Semiconductor packaging – technology benchmark overview

	TSV interposer	Si bridge	Si-IF	Organic interposer	Chip-last fan-out	Glass interposer	TSV Micro bump	TSV Hybrid bonding	Non TSV PoP	Monolithic 3D
Status										
Dielectric constant										
IO pitch (um)										
Interconnect length (mm)										
Interconnect density (IO/mm/layer)										
V_{swing} (V)										
Ron/CTX/CRX (Ohm/F/F)										
Data rate/IO (Gbps)										
Bandwidth density (Gbps/mm)										
Energy-per-bit (pJ/bit)										

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Advanced semiconductor packaging technology – highlights from key players

TSMC

- TSMC's CoWoS (Chip on Wafer on Substrate) is the leading 2.5D packaging technology favored by top AI companies. TSMC is continuously expanding its CoWoS capacity to meet the rising demand in AI applications.
- As interposer sizes grow larger, TSMC has introduced CoWoS-L (Local Silicon Bridge) to replace the traditional silicon interposer, which struggles beyond the 3.3 reticle limit.
- TSMC is a pioneer in 3D hybrid bonding, leveraging its expertise in front-end silicon manufacturing. This technology has already been adopted in commercial server products, including AMD EPYC processors and MI series.
- TSMC is also developing 3D microbump technology for cost-sensitive applications. By 2025, the company plans to launch SoIC-P technology, featuring face-to-back (F2B) bumped packaging. This will integrate a 0.2-reticle N3 (3nm-class) top die with an N4 (4nm-class) bottom die, connected using 25μm pitch microbumps.
- TSMC is preparing for the rise of optical networks, using its expertise in both 2.5D and 3D packaging to offer platforms for Co-packaged optics, aimed at future HPC and network systems.

Intel

Samsung

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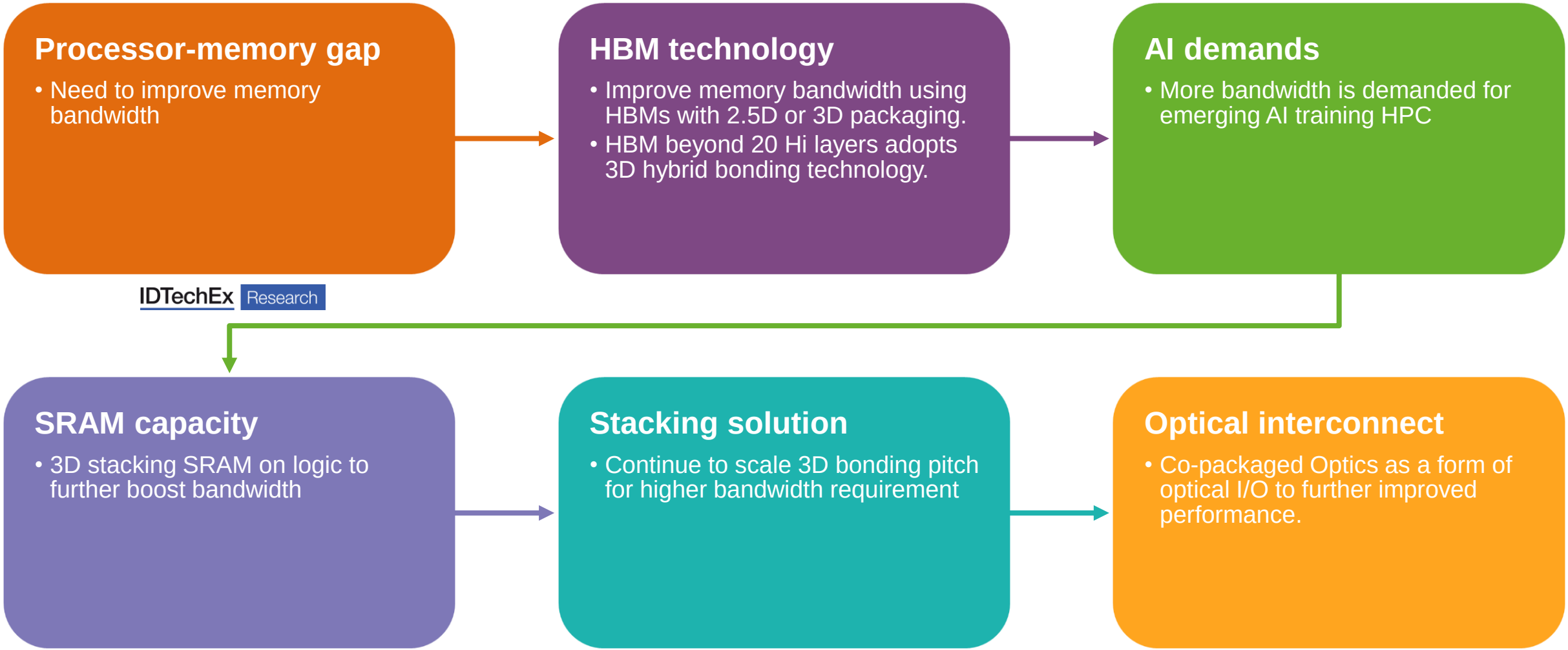
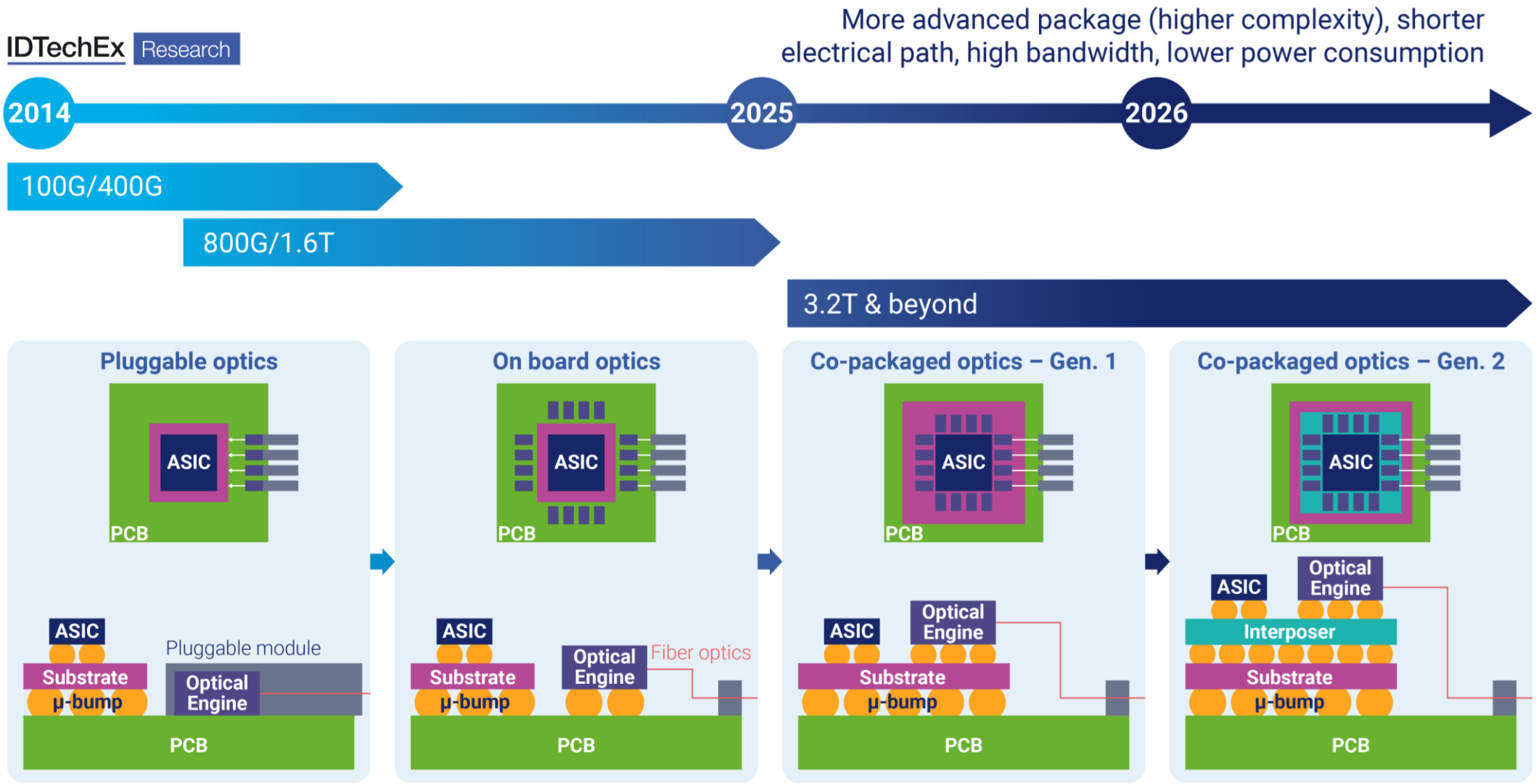
HPC chips integration trend – overview



Key trend of optical transceiver packaging in high-end data centers



Total CPO market

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Total CPO Market Data Table (Revenue)

	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
CPO L2 Switch Revenue (US$ millions)													
AI Interconnect CPO Module Revenue (US$ millions)													

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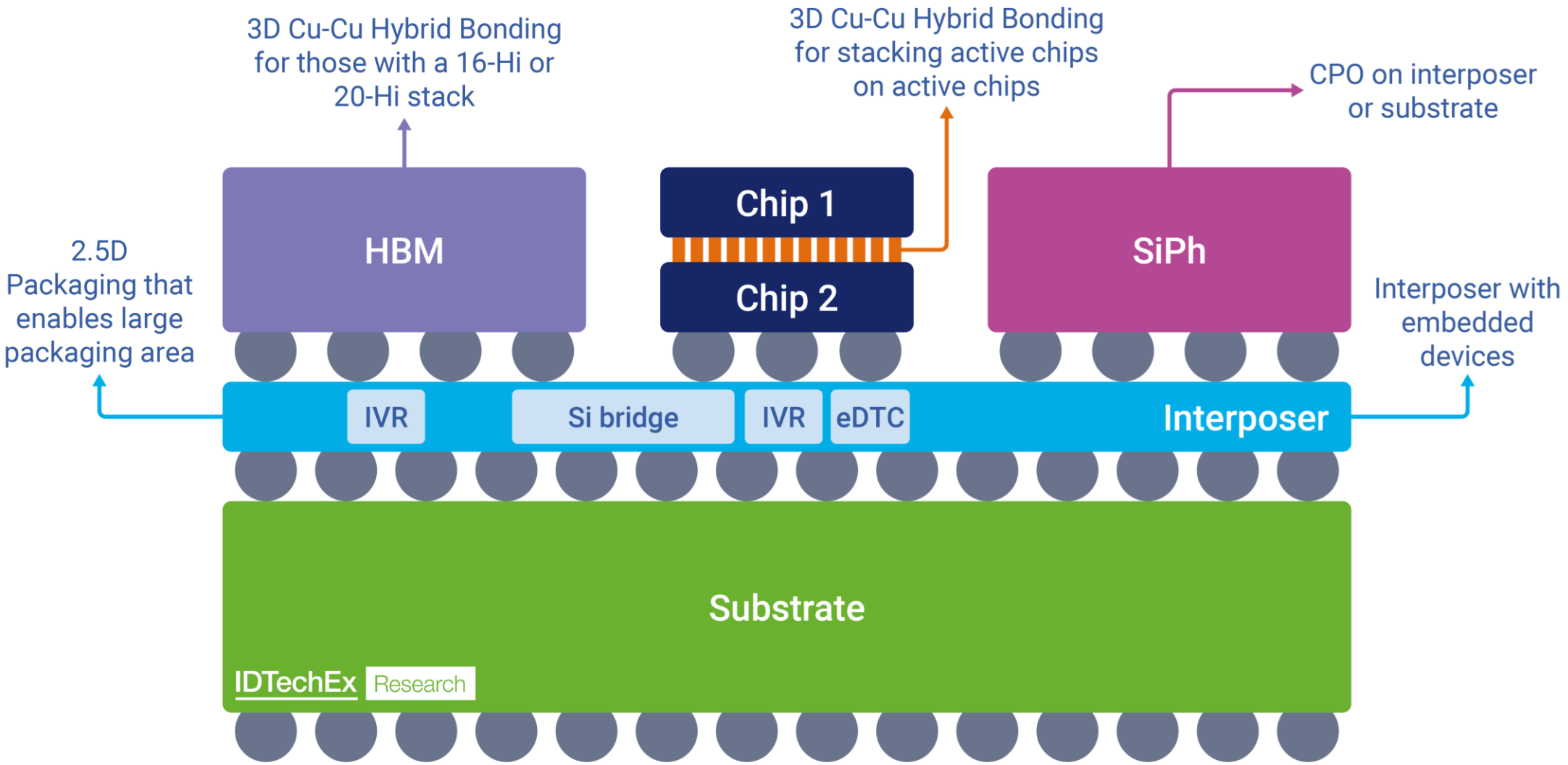
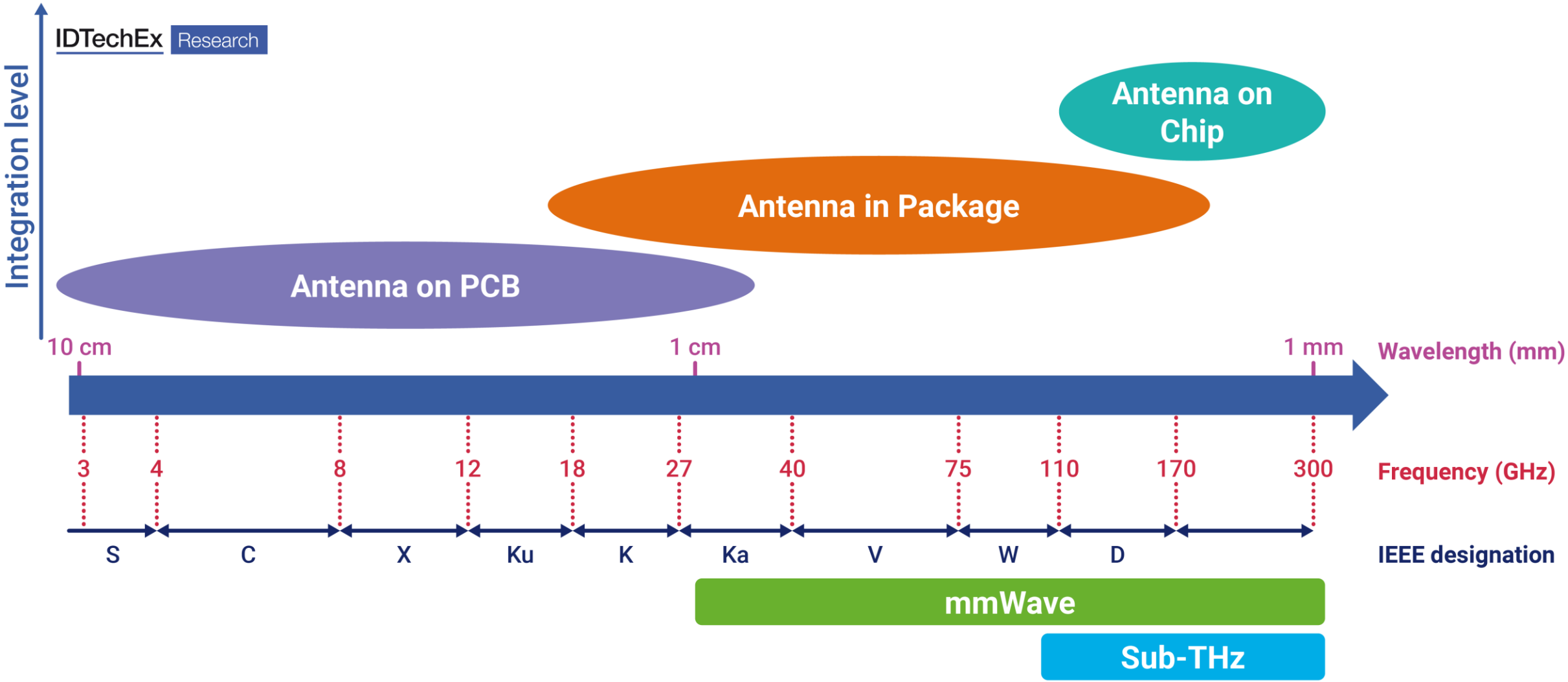
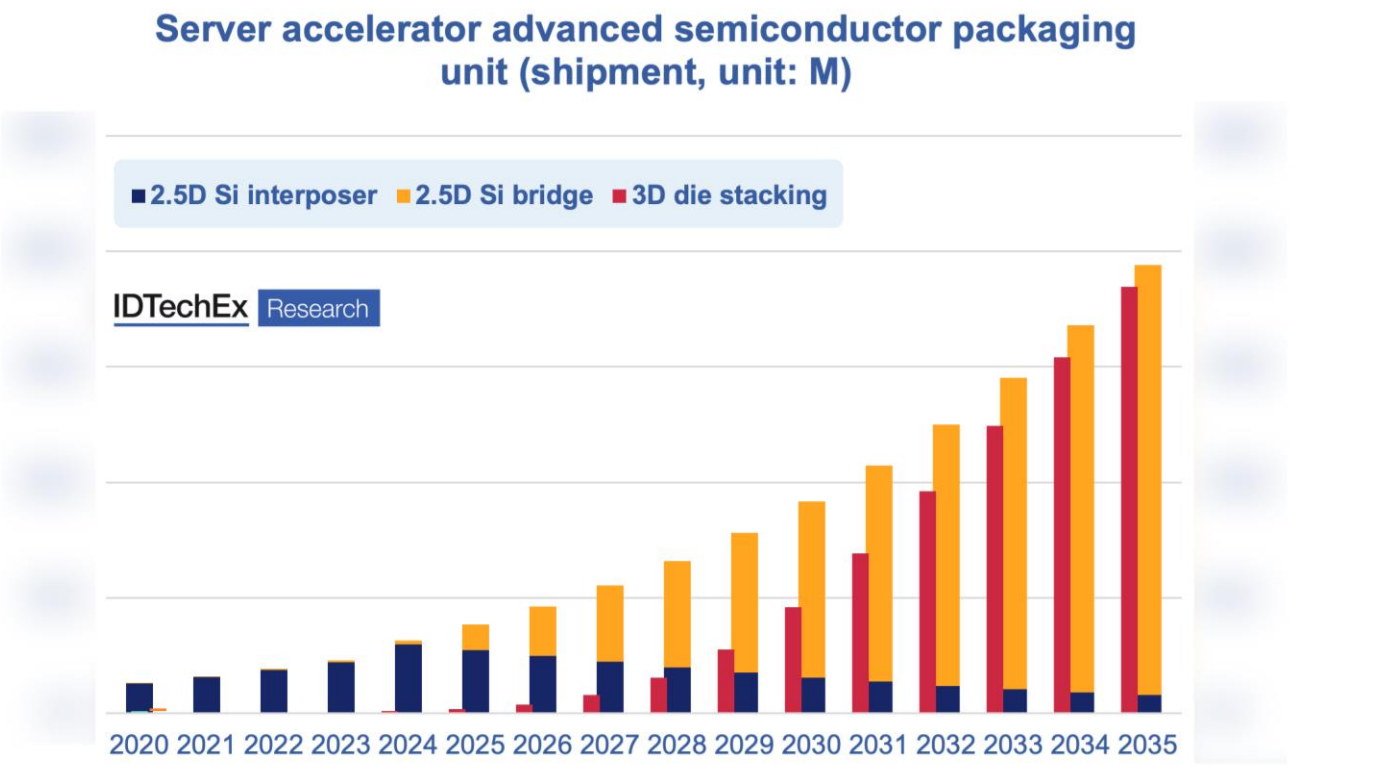
What would the future HPC platform look like?



Overview of antenna packaging technologies vs operational frequency



Data center accelerator: advanced semiconductor packaging unit forecast 2023-2035 (shipment)



Unit Sales (millions)	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035
Advanced packaging total unit													
2.5D Si interposer													
2.5D Si bridge													
3D die stacking													

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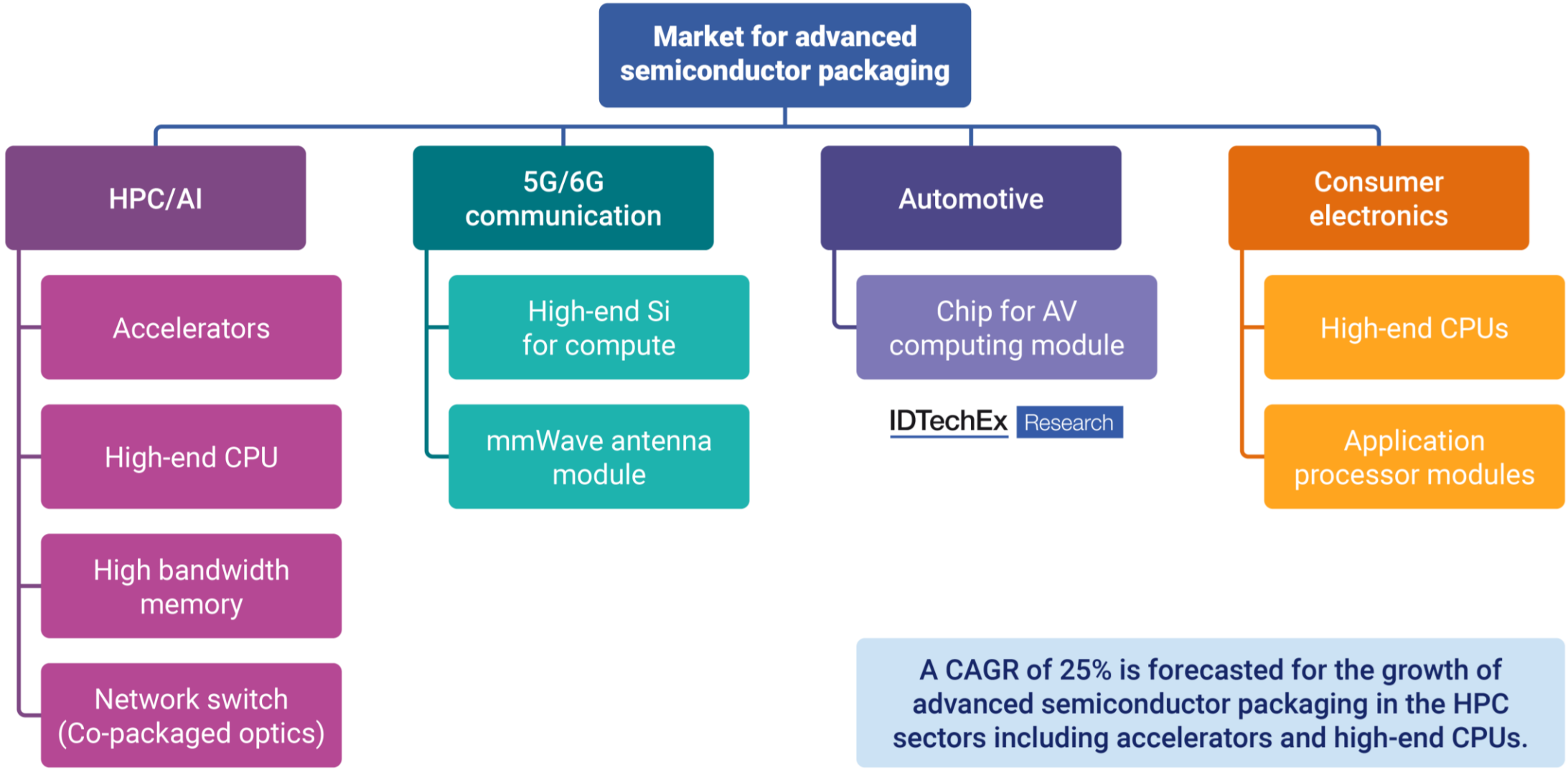
Key markets for advanced semiconductor packaging



A CAGR of 25% is forecasted for the growth of advanced semiconductor packaging in the HPC sectors including accelerators and high-end CPUs.

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